NEC

User's Manual

IE-703079-MC-EM1

In-circuit Emulator Option Board

Target device
V850/SF1™

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
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INTRODUCTION

Target Readers

This manual is intended for users who design and develop application systems using the V850/SF1™.

Purpose

The purpose of this manual is to describe the proper operation of the IE-703079-MC-EM1 and its basic specifications.

Organization

This manual is divided into the following parts.

- Overview
- Names and functions of components
- Cautions

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.
The IE-703079-MC-EM1 is used connected to the IE-703002-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703002-MC when it is connected to the IE-703079-MC-EM1. For the names and functions of parts, and the connection of elements, refer to the **IE-703002-MC User's Manual (U11595E)**.

To learn about the basic specifications and operation methods
→ Read this manual in the order of the **CONTENTS**.

To learn the operation methods and command functions, etc., of the IE-703002-MC and IE-703079-MC-EM1
→ Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numeral representation: Binary ··· xxxx or xxxxB
Decimal ··· xxxx
Hexadecimal ··· xxxxH
Prefix indicating the power of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology

The meanings of terms used in this manual are listed below.

Target device	The device that is targeted for emulation.
Target system	The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.

Related Documents

When using this manual, refer to the following manuals.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ **Documents related to development tools (user's manuals)**

Document Name		Document Number
IE-703002-MC In-circuit emulator		U11595E
IE-703079-MC-EM1 In-circuit emulator option board		U15447E
CA850 C Compiler package Ver. 2.40 or later	Operation	U15024E
	C Language	U15025E
	Project Manager	U15026E
	Assembly Language	U15027E
ID850 Integrated debugger Ver.2.40 Windows™ based	Operation	To be prepared
SM850 System simulator Ver.2.40 Windows based	Operation	To be prepared
SM850 System simulator Ver.2.00 or later	External Part User Open Interface Specifications	U14873E
RX850 Real-time OS Ver.3.13 or later	Basics	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro Real-time OS Ver.3.13	Basics	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 Task debugger Ver.3.01		U13737E
RD850 Pro Task debugger Ver.3.01		U13916E
AZ850 System performance analyzer Ver.3.0		U14410E

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CHAPTER 1 OVERVIEW

The IE-703079-MC-EM1 is an option board for the IE-703002-MC in-circuit emulator. By connecting the IE-703079-MC-EM1 and IE-703002-MC, hardware and software can be debugged efficiently in system development using the V850/SF1.

In this manual, the basic setup procedure and switch settings of the IE-703002-MC when connecting the IE-703079-MC-EM1 are described. For the names and functions of the parts of the IE-703002-MC, and for the connection of elements, refer to the **IE-703002-MC User's Manual (U11595E)**.

1.1 Hardware Configuration

Optional hardware

In-circuit emulator (IE-703002-MC)

Option board (IE-703079-MC-EM1)	By adding this board, the IE-703002-MC can be used as in-circuit emulator for V850/SF1.

Optional hardware

Extension probe SWEX-100SD (for GC/GF package)[Note 1] GF-N17DT (for GF package)[Note 1]	General-purpose extension probe made by TOKYO ELETECH CORPORATION
PC interface board IE-70000-PC-IF-C[Note 2] IE-70000-98-IF-C[Note 2] IE-70000-PCI-IF-A IE-70000-CD-IF-A	This board is used to connect the IE-703002-MC to a personal computer. This board is inserted in the expansion slot of the personal computer. IE-70000-PC-IF-C: for IBM PC/AT™ compatible ISA bus IE-70000-98-IF-C: for PC-9800 series C bus IE-70000-PCI-IF-A: for PCI bus IE-70000-CD-IF-A: for PCMCIA socket
Network module (IE-70000-MC-SV3)	This module is used when a workstation controls the IE-703002-MC via Ethernet™.
Power adapter (IE-70000-MC-PS-B)	AC adapter for in-circuit emulator made by NEC Corporation.

Notes 1. For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

2. Cannot be used for PC98-NX series

1.2 Features (When Connected to IE-703002-MC)

- Maximum operating frequency: 16 MHz (at 5.0 V operation)
- Extremely lightweight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- The following pins can be masked.
  $\overline{\text{RESET}}$, NMI, $\overline{\text{WAIT}}$, $\overline{\text{HLDRQ}}$
- Two methods of connection to target system:
  - Pod tip direct connection (For information on the pod, refer to the **IE-703002-MC User's Manual (U11595E)**)
  - Attach an extension probe (sold separately) to the pod tip for connection
- The dimensions of the IE-703079-MC-EM1 are as follows.

Parameter		Value
Power consumption (Max. value at 5.0 V supply voltage)		2.5 W (at 16 MHz operation frequency)[Note]
External dimensions (Refer to **APPENDIX PACKAGE DRAWINGS**)	Height	50 mm
	Length	130 mm
	Width	252 mm
Weight		300 g

Note 12.5 W when IE-703002-MC connected to IE-703079-MC-EM1

1.3 Function Specifications (When Connected to IE-703002-MC)

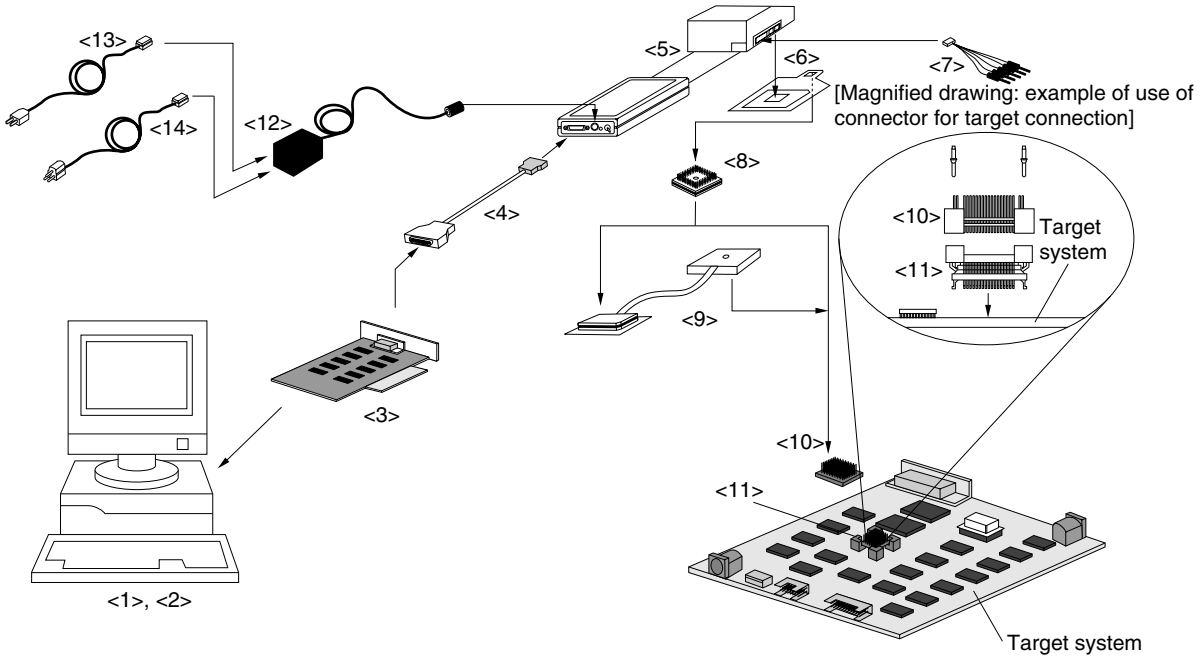
Parameter			Specification
Emulation memory capacity	Internal ROM		256 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB
Coverage memory capacity for execution/pass detection	Internal ROM		256 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB
Coverage memory capacity for memory access detection	External memory		1 MB
Coverage memory capacity for branching entry number counting	Internal ROM		256 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB

Caution Some of the functions may not be supported, depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703002-MC to the IE-703079-MC-EM1 and a personal computer (PC-9800 series or PC/AT (or compatibles)) is shown below.

Figure 1-1. System Configuration



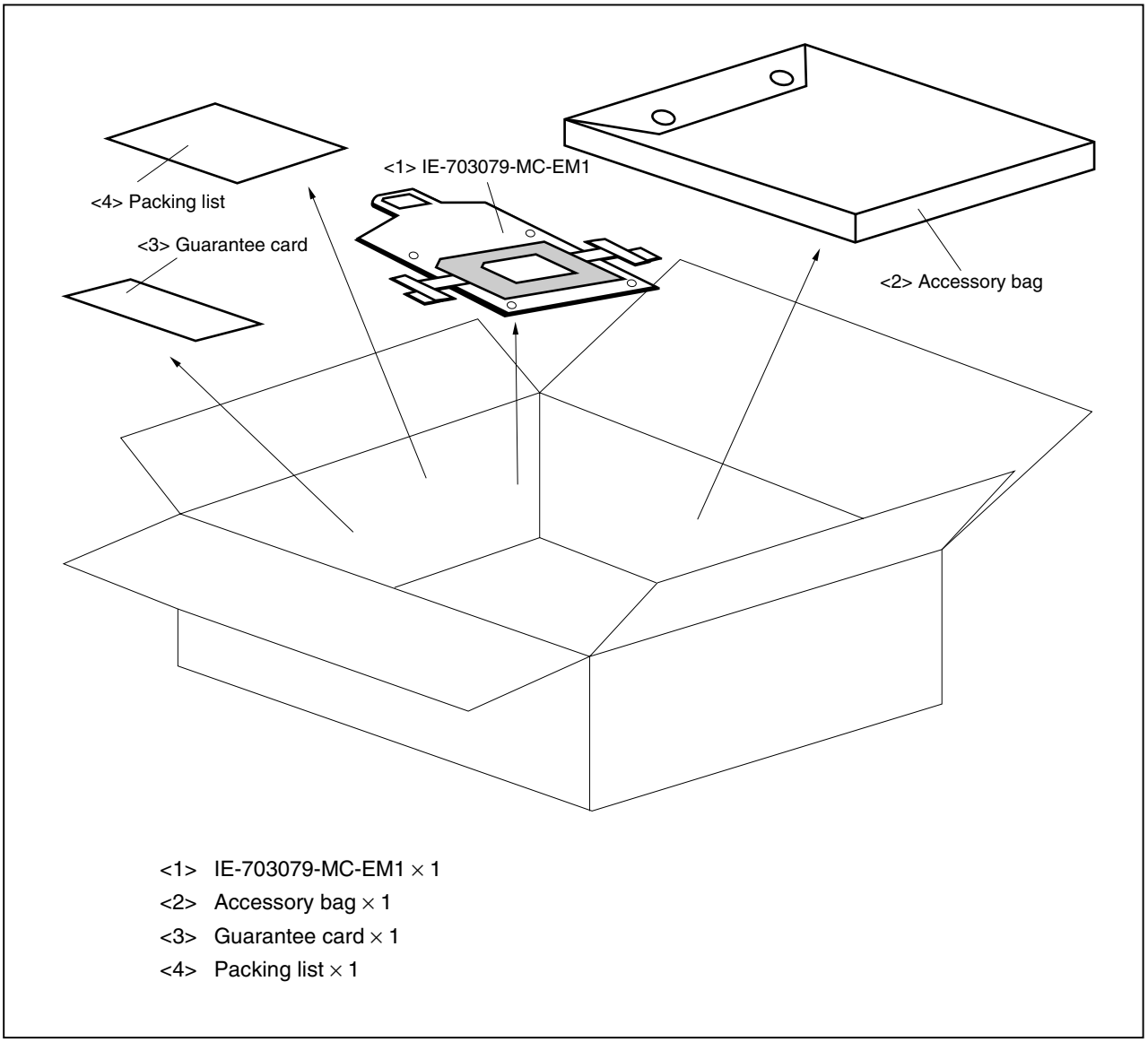
Remark

<1> Personal computer (PC-9800 series or PC/AT or compatibles)
<2> Debugger (ID850: sold separately)
<3> PC interface board
(IE-70000-98-IF-C/IE-70000-PC-IF-C, IE-70000-PCI-IF-A/IE-70000-CD-IF-A: sold separately)
<4> PC interface cable (included with IE-703002-MC)
<5> In-circuit emulator (IE-703002-MC: sold separately)
<6> In-circuit emulator option board (IE-703079-MC-EM1: this product)
<7> External logic probe (included with IE-703002-MC)
<8> Socket for target connection (YQSOCKET100SDN: sold separately)
<9> Extension probe (for GC package: SWEX-100SD, for GF package: SWEX-100SD/GF-N17DT)
<10> Connector for emulator connection (YQPACK100SD: included)
<11> Connector for target connection (NQPACK100SD: included)
<12> Power adapter (IE-70000-MC-PS-B: sold separately)
<13> AC100V power cable (sold separately: included with IE-70000-MC-PS-B)
<14> AC220V power cable (sold separately: included with IE-70000-MC-PS-B)

1.5 Contents in Carton

The carton of the IE-703079-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and the connector accessories. If there are missing or damaged items, please contact an NEC sales representative or an NEC distributor.

Figure 1-2. Contents in Carton

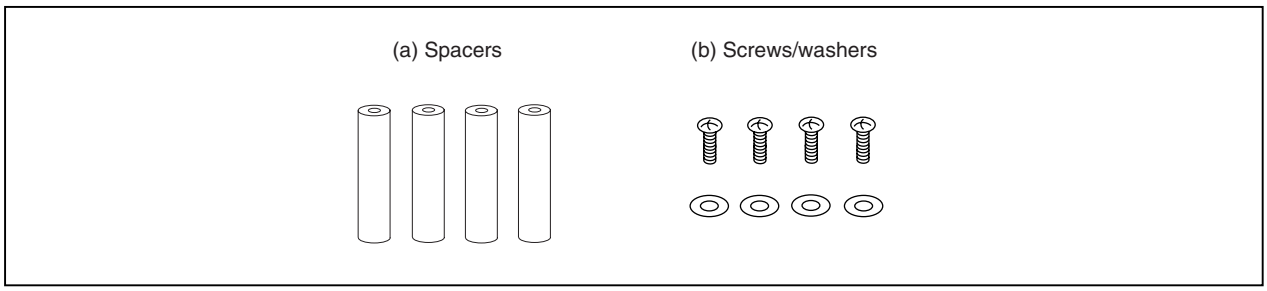


<1> IE-703079-MC-EM1 × 1
<2> Accessory bag × 1
<3> Guarantee card × 1
<4> Packing list × 1

Check that the accessory bag contains this manual, an accessory list (× 1), and the following accessories.

(a) Spacers × 4
(b) Screws/washers × 4 sets
(including screws and washer × 4)

Figure 1-3. Accessories



1.6 Connection Between IE-703002-MC and IE-703079-MC-EM1

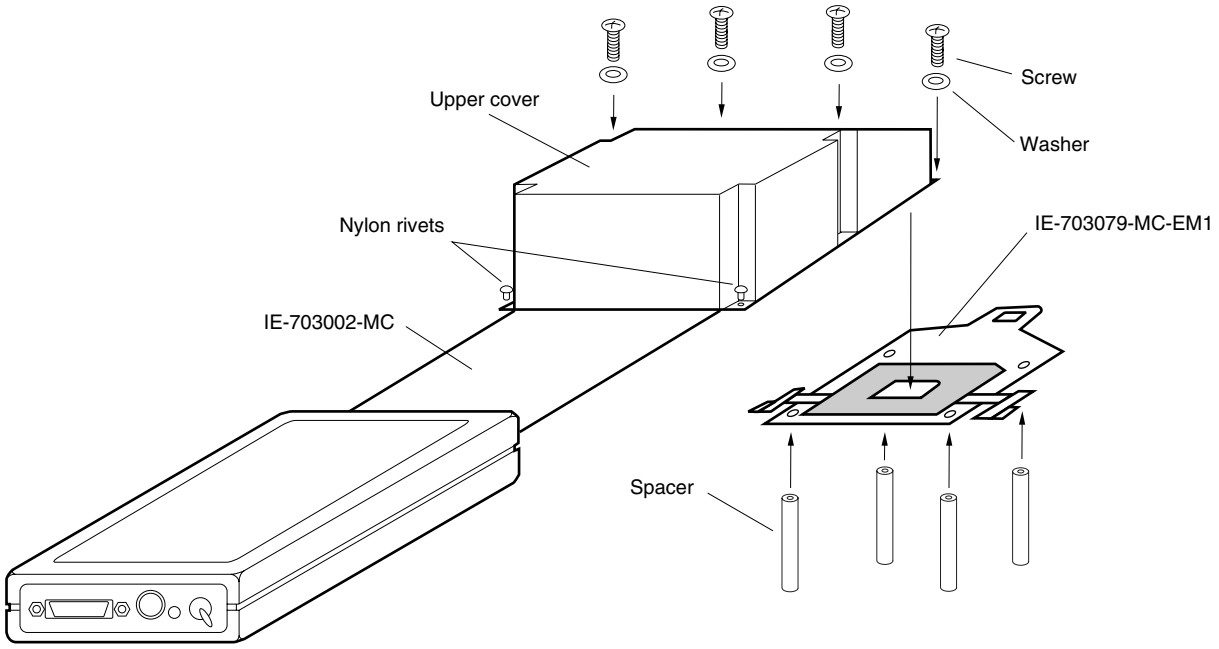
The procedure for connecting the IE-703002-MC and IE-703079-MC-EM1 is described below.

Caution Connect carefully so as not to break or bend connector pins.

<1> Remove the pod cover (upper and lower) of the IE-703002-MC.
<2> Set the PGA socket lever of the IE-703079-MC-EM1 to the OPEN position as shown in Figure 1-4 (b).
<3> Connect the IE-703079-MC-EM1 to the PGA socket at the back of the IE-703002-MC pod (refer to Figure 1-4 (c)). When connecting, position the IE-703002-MC and IE-703079-MC-EM1 so that they are horizontal.
<4> Set the PGA socket lever of the IE-703079-MC-EM1 to the CLOSE position as shown in Figure 1-4 (b).
<5> Set the IE-703002-MC pod jumpers (JP1 to JP3).
The factory settings of JP2 are pins 1 and 2 shorted.
<6> Place the supplied spacers in the four corner holes of the IE-703079-MC-EM1. Fix the spacers with the supplied screws.
<7> Fix the IE-703002-MC pod cover (upper) end with nylon rivets.

Figure 1-4. Connection Between IE-703002-MC and IE-703079-MC-EM1 (1/2)

(a) Overview



(b) PGA socket lever of IE-703079-MC-EM1

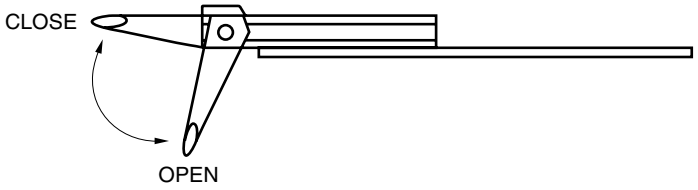
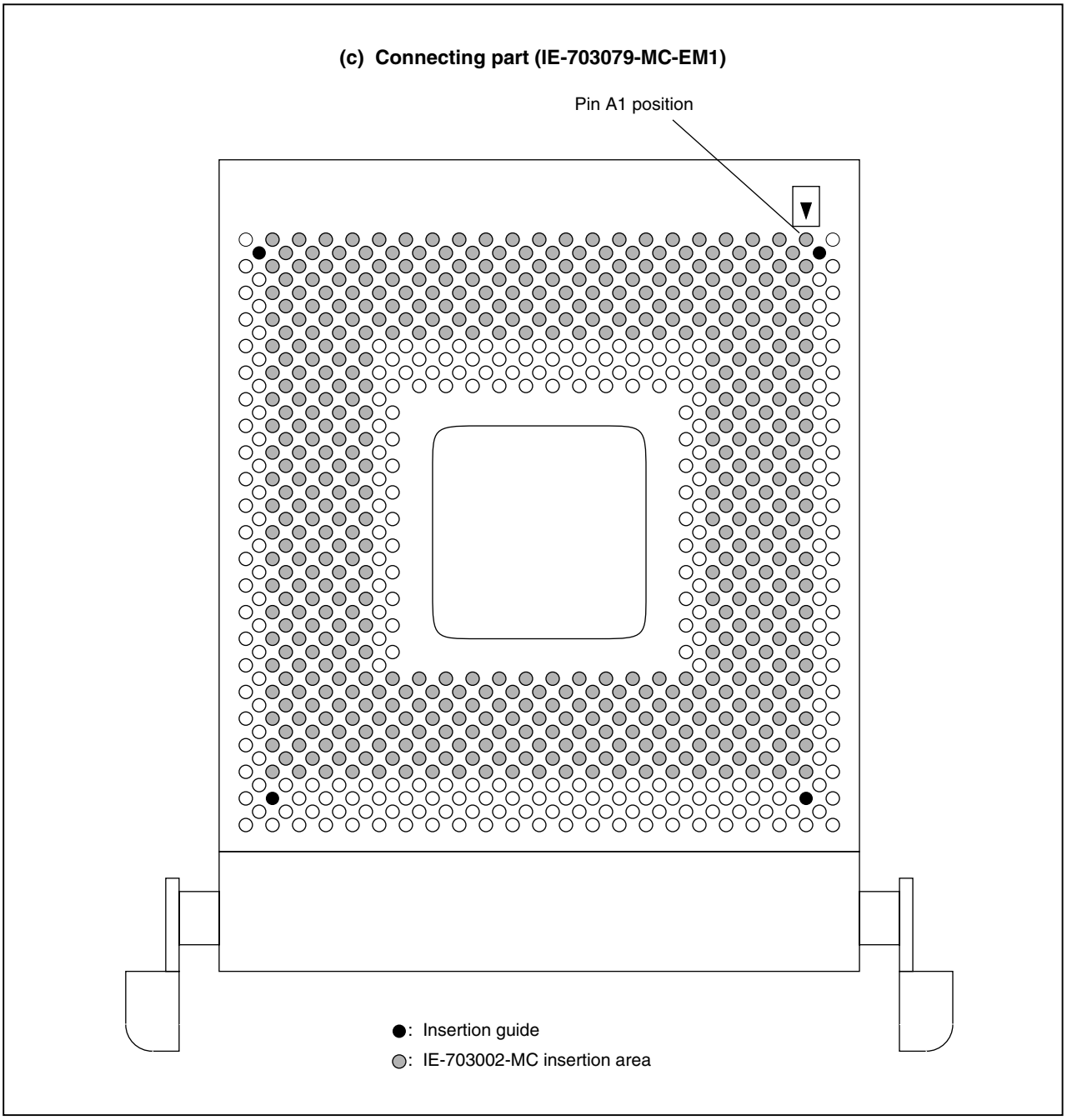


Figure 1-4. Connection Between IE-703002-MC and IE-703079-MC-EM1 (2/2)

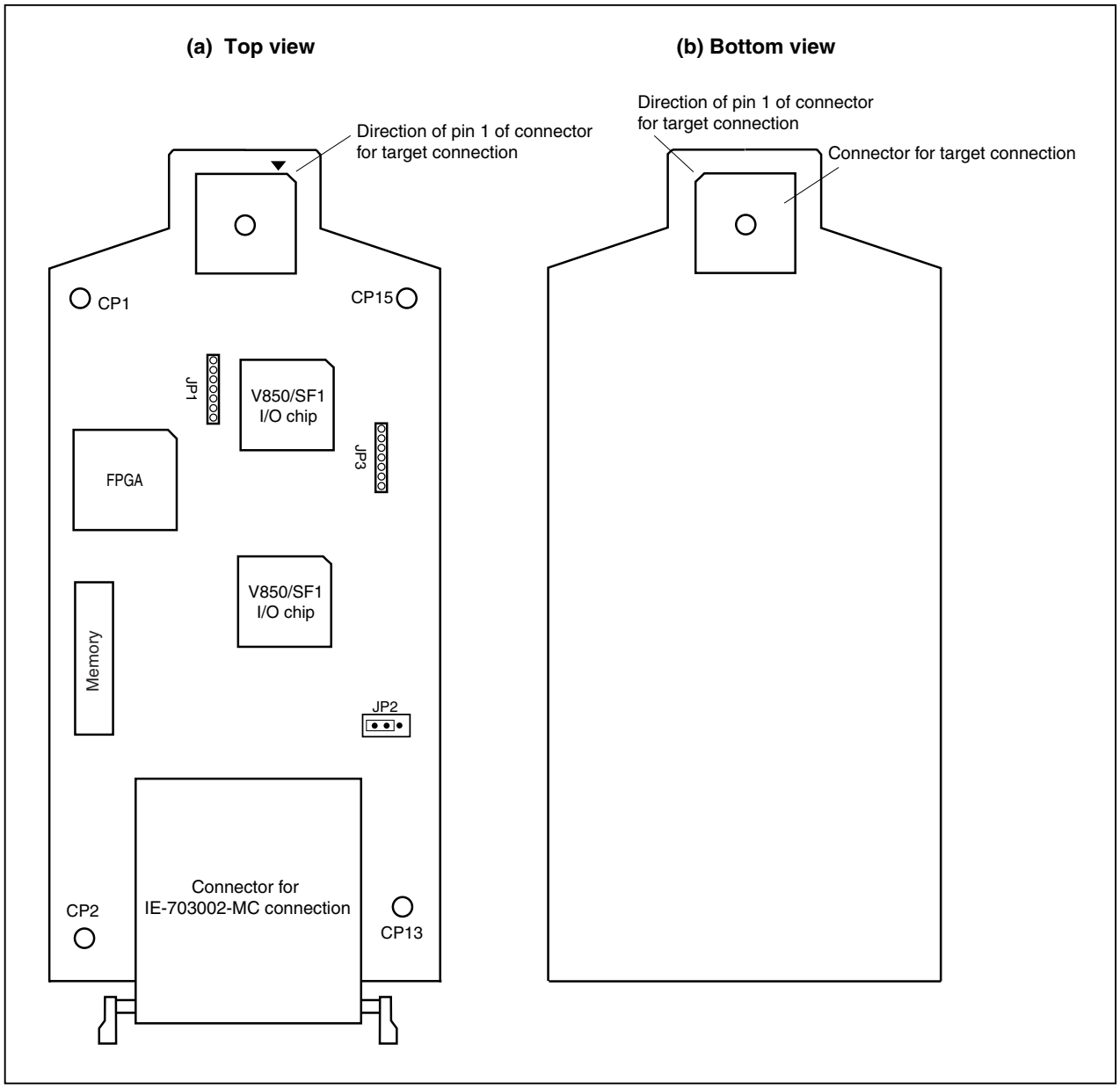


CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names, functions, and switch settings of components in the IE-703079-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-703002-MC User's Manual (U11595E)**.

2.1 Component Names and Functions of IE-703079-MC-EM1

Figure 2-1. IE-703079-MC-EM1



(1) TEST pins (CP1, CP2, CP13, CP15)

These are pins used for testing the analog signals of the standalone emulator.

- CP1: GND
- CP2: GND
- CP13: GND
- CP15: GND

(2) JP1

This is a pin board for supplying the main system clock.

(3) JP2

This is the switch jumper for the main system clock supply source. Use and retain the factory settings (pins 1 and 2 shorted).

(4) JP3

This is a pin board for supplying the subsystem clock (for details, refer to **2.2 Clock Settings**).

(5) Connector for IE-703002-MC connection

This is a connector for connecting with the IE-703002-MC.

(6) Connector for target connection

This is a connector for connecting with the target system or the extension probe.

2.2 Clock Settings

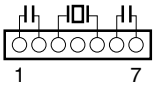
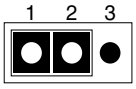
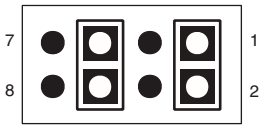
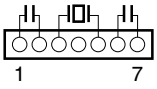
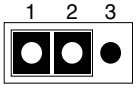
This section describes the clock settings.

For the position of the JP1 and JP2 in the IE-703079-MC-EM1, refer to Figure 2-1.

For the jumper switch position in the IE-703002-MC, refer to the **IE-703002-MC User's Manual (U11595E)**.

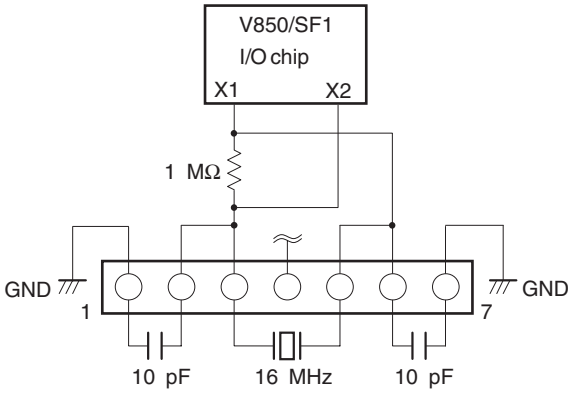
2.2.1 Main system clock setting

Table 2-1. Main System Clock Setting

Emulator Use Environment	Clock Supply Method	IE-703079-MC-EM1 Setting		IE-703002-MC Setting		
		JP1	JP2	SW1	SW2	JP2
When using emulator as standalone unit	Internal clock			ON	OFF	
When using emulator with target system	Internal clock					

Caution Emulation cannot be performed by inputting a clock from the target board.

The specifications of JP1 are as follows.



2.2.2 Subsystem clock setting

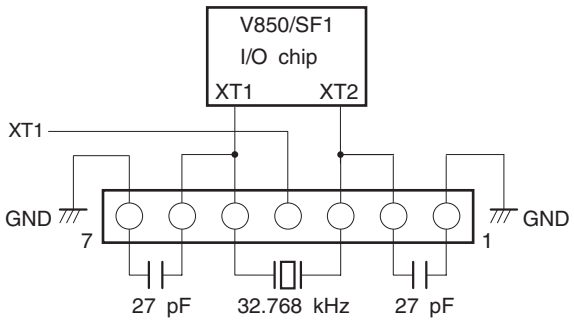
Table 2-2. Subsystem Clock Setting

Emulator Use Environment	Clock Supply Method	IE-703079-MC-EM1 Setting
		JP3
When using emulator as standalone unit	Internal clock[Note 1]	Oscillator mounted (a 32.768 kHz oscillator is mounted when shipped)[Note 2]
When using emulator with target system	Internal clock[Note 1]	Oscillator mounted (a 32.768 kHz oscillator is mounted when shipped)[Note 2]

Notes 1. The internal clock does not support the clock input by an oscillator.

2. To use a subsystem clock frequency other than 32.768 kHz, remove the resonator on JP3 and mount any oscillator.

The specifications of JP3 are as follows.

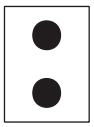


Caution Emulation cannot be performed by inputting a clock from the target board.

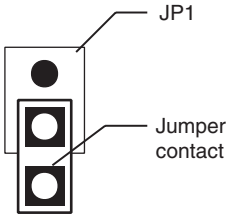
2.3 Illegal Access Detection ROM Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SF1 by connecting the IE-703079-MC-EM1, set JP1 of the IE-703002-MC as follows.

Table 2-3. JP1 Setting in IE-703002-MC

JP1		Description
Open[Note]		Illegal access detection ROM (mounted on IE-703079-MC-EM1) for V850/SF1 is used.

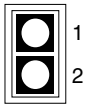
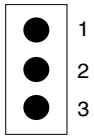
Note When JP1 is set open, keep the removed jumper contact attached to one pin as shown in the drawing on the right.



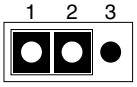
2.4 CPU Operation Voltage Range Switching Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SF1 by connecting the IE-703079-MC-EM1, set JP3 and JP4 of the IE-703002-MC as follows.

Table 2-4. JP3 and JP4 Setting in IE-703002-MC

JP3, JP4		Description
JP3	 (Short)	The operation voltage range of the IE-703002-MC is 3.0 to 5.5 V.
JP4	 (Open)	The power supply for PORTV_{DD} is generated on the IE-703079-MC-EM1.

CHAPTER 3 FACTORY SETTINGS

Item	Description	Remark
JP1	Oscillator mounted	16 MHz clock supplied for main system clock
JP2[Note]	1 2 3  (1-2 Shorted)	Internal clock used for main system clock
JP3	Oscillator mounted	32.768 kHz clock supplied for subsystem clock

Note Use JP2 with the factory settings.

CHAPTER 4 CAUTIONS

4.1 V_{DD0} and $PORTV_{DD}$ of Target System

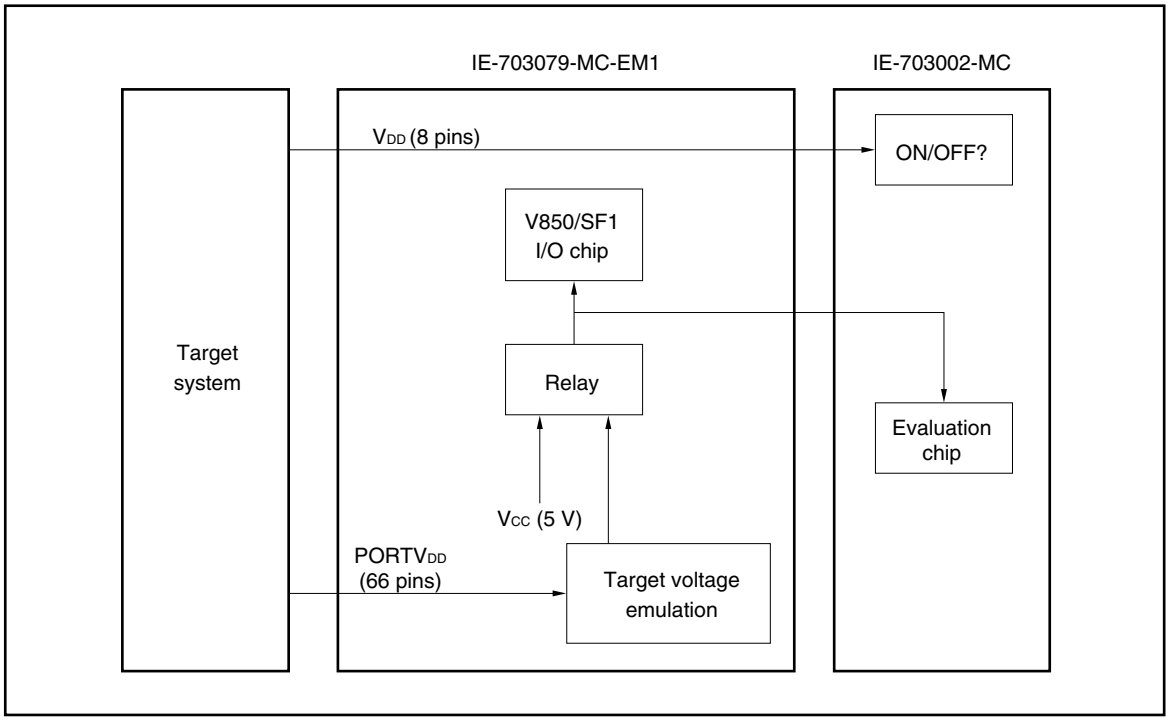
(1) V_{DD0} in the target system is used to sense the level for target system power supply ON/OFF.

- When V_{DD0} is lower than 1 V, it is judged that the target system is not connected, and mapping of the target memory cannot be performed with a debugger (FCAN cannot be used).
- When V_{DD0} is 1 V or higher, it is judged that the target system is connected, and mapping of the target memory can be performed with a debugger (FCAN can be used).

(2) $PORTV_{DD}$ in the target system is not supplied directly to the emulator chip; it is connected to the target voltage emulation circuit.

- When $PORTV_{DD}$ is lower than 3 V, V_{CC} (5 V) in the internal emulator is supplied to the emulator chip.
- When $PORTV_{DD}$ is 3 V or higher, a voltage of the same potential as $PORTV_{DD}$ in the target system is generated and supplied to the emulator chip.

Figure 4-1. Schematic Diagram of Power Supply Acquisition

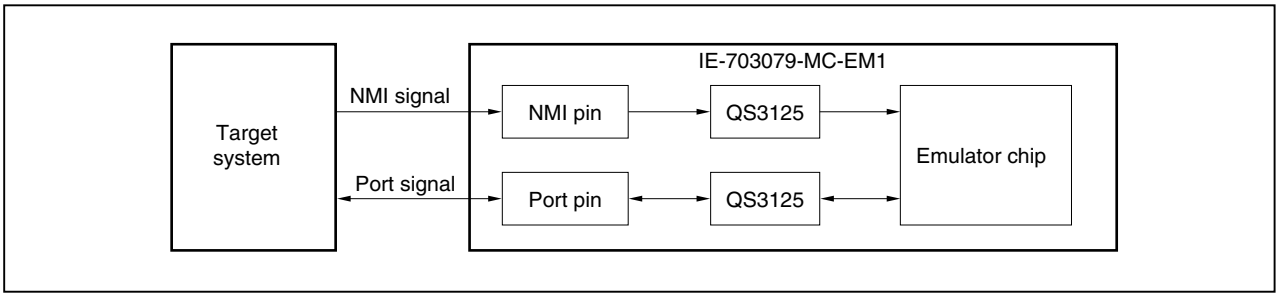


4.2 NMI Signal

The input signal (NMI signal) from the target system is delayed (t_{pD} = 0.25 ns (TYP.)) because it passes through QS3125 (Q switch), and I/O signals (ports 4, 5, 6, 9, 11) pass through QS3384 (Q switch) before it is input to the emulator chip.

In addition, the DC characteristics change. The input voltage becomes V_{IH} = 2.0 V (MIN.), V_{IL} = 0.8 V (MAX.), and the input current becomes I_{IN} = ±0.5 μA (MAX.).

Figure 4-2. NMI Signal Flow Path



4.3 V_{PP} Signal

The V_{PP} signal from the target system is left open in the emulator.

4.4 NMI Signal Mask Function

When using the P00/NMI pin in the port mode, do not mask the NMI signal.

4.5 Bus Interface Pin

The operation of the pin for the bus interface differs between the emulator and the target device as follows.

Table 4-1. Bus Interface Pin Operation List (1/2)

(a) During break

Pin Name	Internal Memory								External Memory			
	Memory Used by Emulator			Internal ROM	Internal RAM		Internal Peripheral I/O		Emulation RAM		Target System	
	F	R	W	R	R	W	R	W	R	W	R	W
A16 to A21	Hold the last accessed address								Active		Active	
AD0 to AD15	Hi-Z								Active		Active	
ASTB	H								Active		Active	
R/$\overline{W}$	H								Active		Active	
$\overline{DSTB}$	H								H		Active	
$\overline{LBEN}$	H								Active		Active	
$\overline{UBEN}$	H								Active		Active	
$\overline{WAIT}$	Invalid								Maskable		Maskable	
$\overline{HLDRQ}$	Maskable								Maskable		Maskable	
$\overline{HLDAK}$	H or L								H or L		H or L	
$\overline{WRL}$	H								H		H	**Note**
$\overline{WRH}$	H								H		H	**Note**
$\overline{RD}$	H								H		**Note**	H

Note Active

Caution When accessing an FCAN register with the external memory expanded, a bus cycle for FCAN access is generated in AD0 to AD15 and A16 to A21. However, R/$\overline{W}$, $\overline{DSTB}$, $\overline{LBEN}$, $\overline{UBEN}$, $\overline{WRL}$, $\overline{WRH}$, and $\overline{RD}$ are inactive.

Remarks 1. F: Fetch
R: Read
W: Write

2. H: High-level output
L: Low-level output
Hi-Z: High-impedance

Table 4-1. Bus Interface Pin Operation List (2/2)

(b) During run

Pin Name	Internal Memory							External Memory					
	Internal ROM		Internal RAM			Internal Peripheral I/O		Emulation RAM			Target System		
	F	R	F	R	W	R	W	F	R	W	F	R	W
A16 to A21	Hold the last accessed address							Active			Active		
AD0 to AD15	Hi-Z							Active			Active		
ASTB	H							Active			Active		
R/$\overline{W}$	H							Active			Active		
$\overline{DSTB}$	H							H			Active		
$\overline{LBEN}$	H							Active			Active		
$\overline{UBEN}$	H							Active			Active		
$\overline{WAIT}$	Invalid							Maskable			Maskable		
$\overline{HLDRQ}$	Maskable							Maskable			Maskable		
$\overline{HLDAK}$	H or L							H or L			H or L		
$\overline{WRL}$	H							H			H		**Note**
$\overline{WRH}$	H							H			H		**Note**
$\overline{RD}$	H							H			**Note**		H

Note Active

Caution When accessing an FCAN register with the external memory expanded, a bus cycle for FCAN access is generated in AD0 to AD15 and A16 to A21. However, R/$\overline{W}$, $\overline{DSTB}$, $\overline{LBEN}$, $\overline{UBEN}$, $\overline{WRL}$, $\overline{WRH}$, and $\overline{RD}$ are inactive.

Remarks 1. F: Fetch
R: Read
W: Write

2. H: High-level output
L: Low-level output
Hi-Z: High-impedance

CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICE AND TARGET INTERFACE CIRCUIT

Differences between the signal lines of the target device and the signal lines of the IE-703079-MC-EM1 target interface circuit are described in this chapter.

The target device is a CMOS circuit, whereas the target interface circuit of the IE-703079-MC-EM1 is configured with an emulation circuit such as a gate array TTL or CMOS-IC.

When debugging the IE system connected to the target system, the IE system emulates as if the real target device is operating on the target system.

Small differences occur however, because the IE system is emulating actual operation.

(1) Signals input/output to/from the emulation CPU μPD70F3079Y

(2) Other signals

The IE-703079-MC-EM1 circuit regarding the (1) and (2) signals described above is as follows.

(1) Signals input/output to/from the emulation CPU μPD70F3079Y

- P00
- P07/INTP6 to P01/INTP0
- P15/SCK1/ASCK0 to P10/SO0/SDA0
- P27 to P20/SI3/RXD1
- P34/VM45/TI71 to P30/TI2/TO2
- P77/ANI7 to P70/ANI0
- P83/ANI11 to P80/ANI8
- P107/KR7/TO1 to P100/KR0/TO7

(2) Other signals

- NMI
- P47/AD7 to P40/AD0
- P57/AD15 to P50/AD8
- P65/A21 to P60/A16
- P96/$\overline{\text{HLDRQ}}$ to P90/$\overline{\text{LBEN}}$
- P117/CANRX2 to P110/$\overline{\text{WAIT}}$
- X1, XT1
- $\overline{\text{RESET}}$
- CLKOUT
- PORTV_{DD}
- CPUREG
- V_{PP}/MODE
- X2, XT2
- GND0, GND1, GND2, PORTGND

Figure 5-1. Equivalent Circuit of Emulation Circuit (1/5)

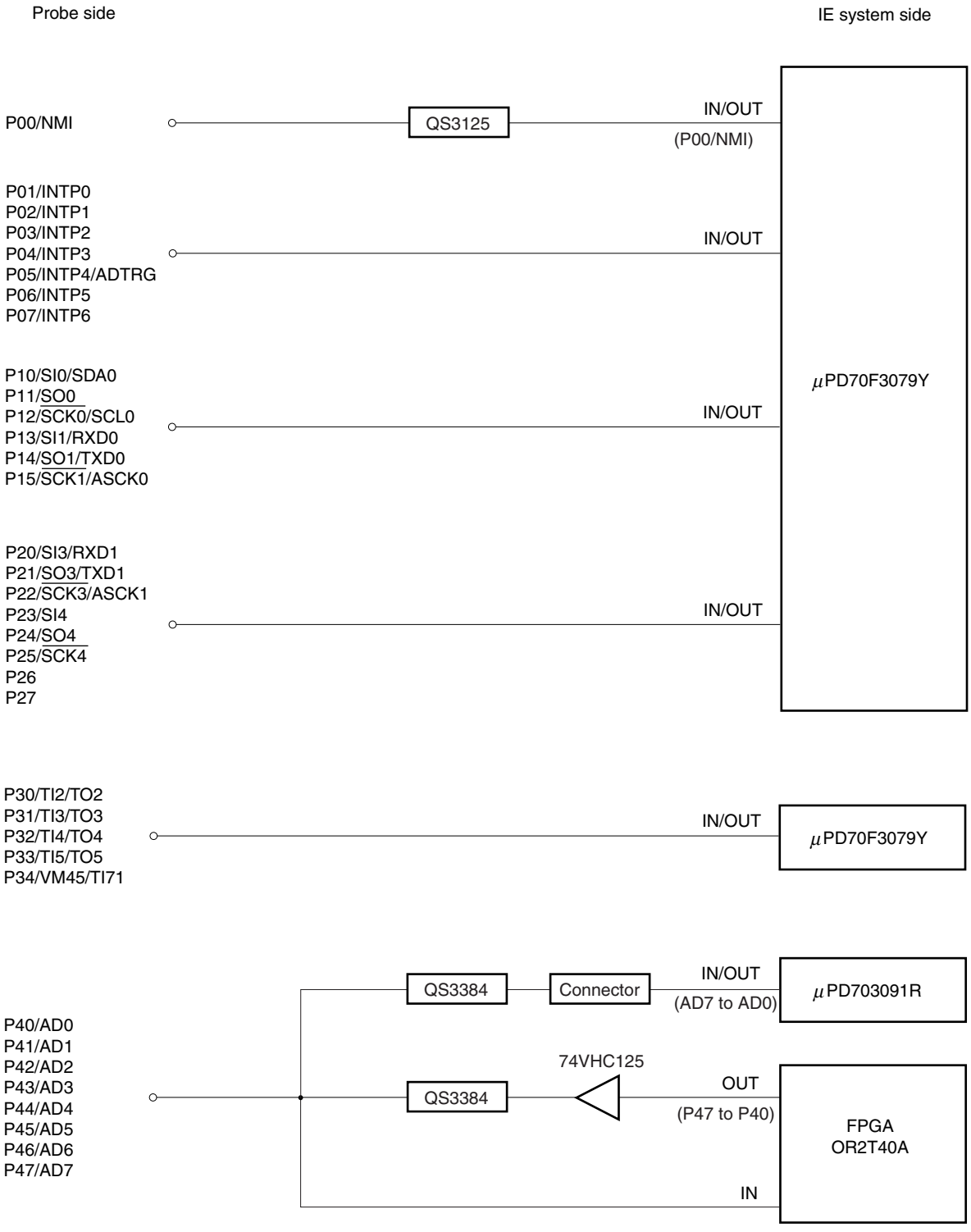


Figure 5-1. Equivalent Circuit of Emulation Circuit (2/5)

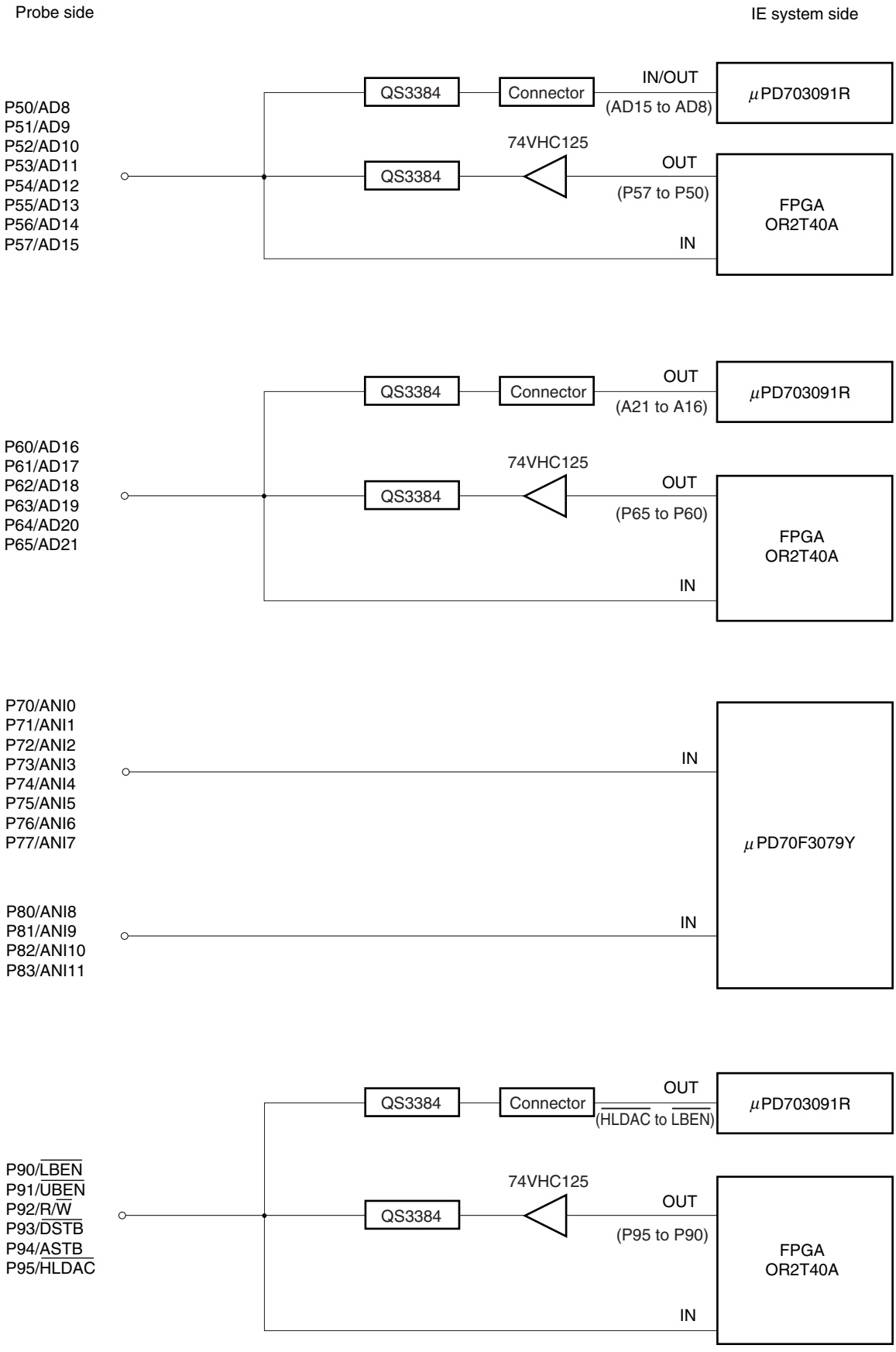


Figure 5-1. Equivalent Circuit of Emulation Circuit (3/5)

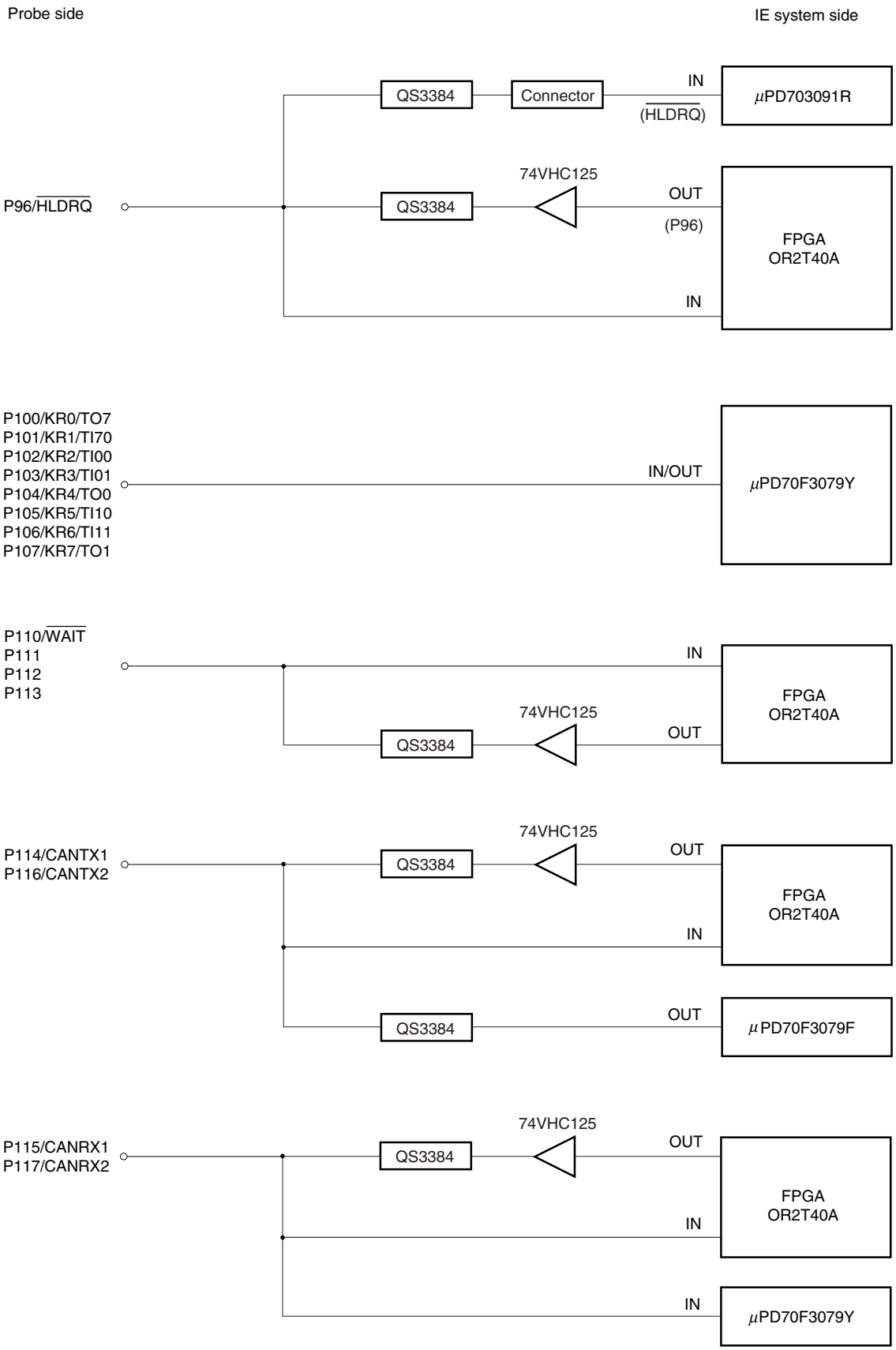


Figure 5-1. Equivalent Circuit of Emulation Circuit (4/5)

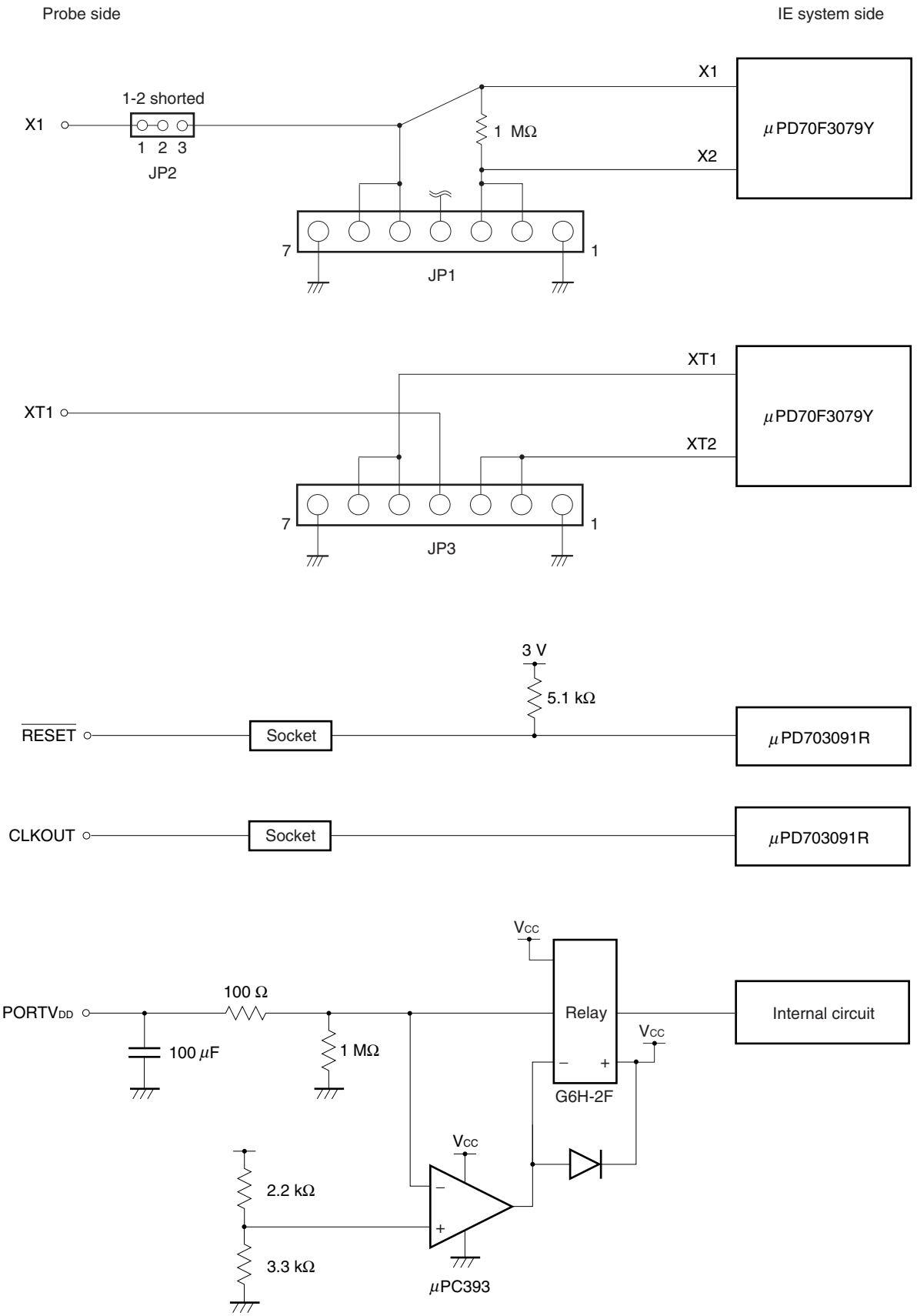
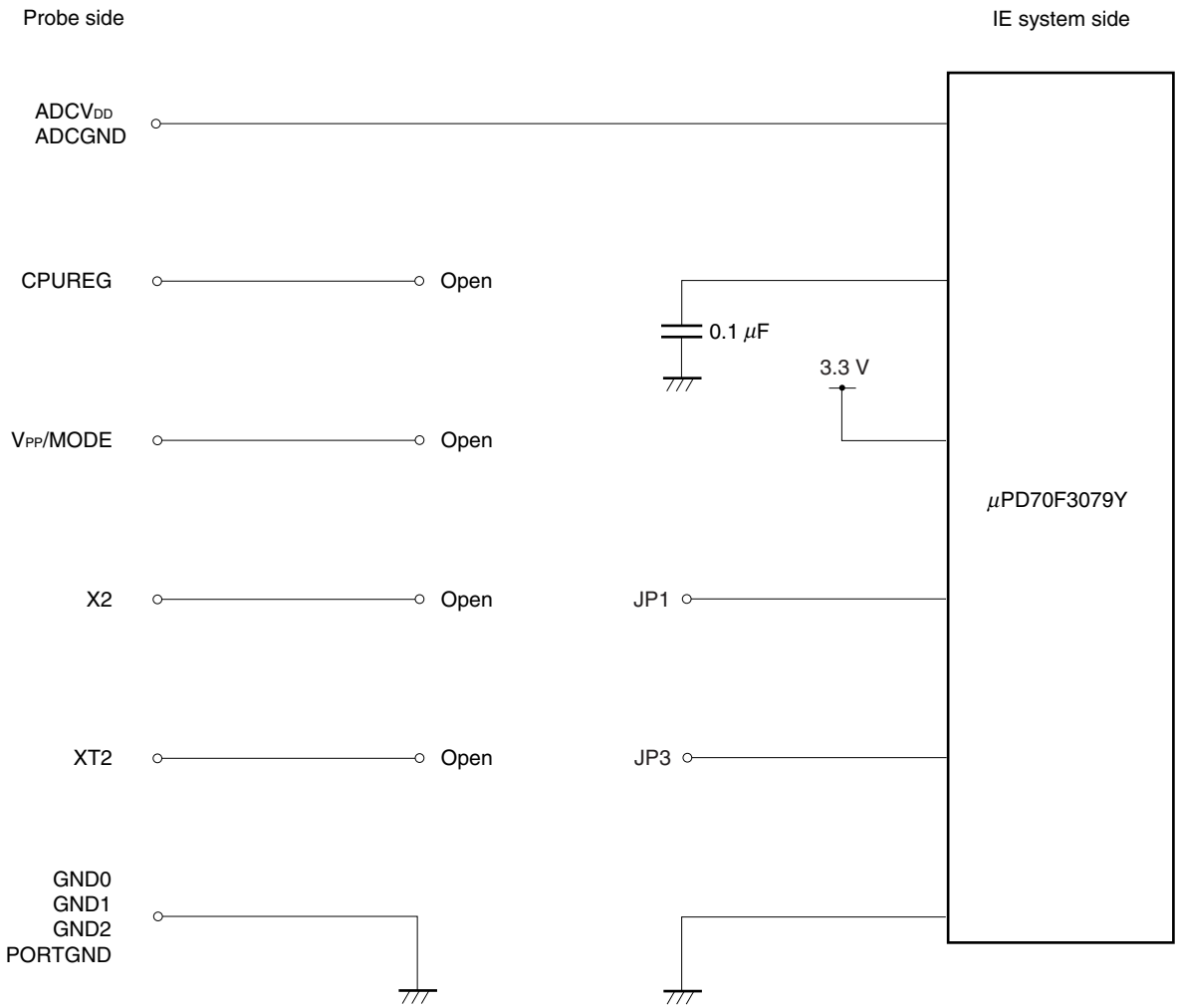
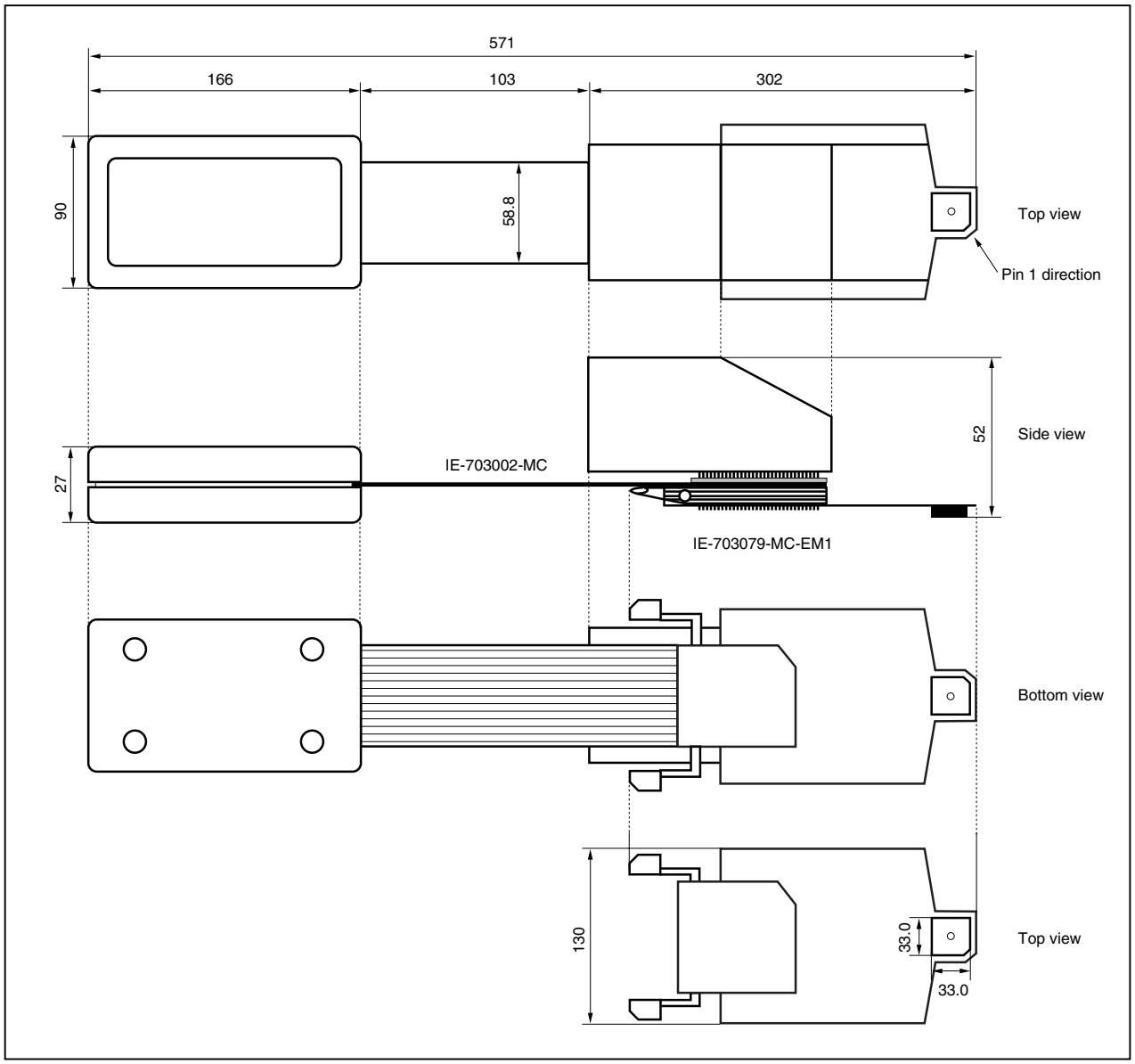


Figure 5-1. Equivalent Circuit of Emulation Circuit (5/5)



APPENDIX PACKAGE DRAWINGS

IE-703002-MC + IE-703079-MC-EM1 (Unit: mm)



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